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EXAMINER	
RIAD, AMINE	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,097	KUO, HUNG-YU	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *5 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claims 1-20 have presented for examination.

Claims 1-20 have been rejected.

Claims 5 and 15 have been canceled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-6, 8,11-13, 15-16, 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson US Patent 6,003,130.

In regard to claims 1, and 11 Anderson discloses:

- method of initializing a computer system equipped with a debugging system (Figure 2; item 33),
- the computer system has a CPU (Figure 2; item12), local bus (Figure 2; item 16), peripheral bus (Figure 2; item 60 and 70) and expansion buses (Figure 2; item 72), a first (Figure 2; item 14 " the system controller 14 also connects the CPU

bus 16 to a PCI bus 60") and second bridges (Figure 2; item 30), and a ROM coupled to the expansion bus and storing a first BIOS code (Figure 2; item 80),

,and wherein the debugging system is coupled to the peripheral bus, the method comprising the steps of:

- operating the CPU in a normal mode wherein first data requests directed to the ROM are routed to the local bus by the CPU; (Figure 3; item 92)["CPU 12 executes a startup routine that is also stored in the EEPROM 80 along with the BIOS program" step 92 defines normal mode]

- operating the CPU in a debugging mode wherein second data requests directed to the debugging system are routed to the local bus by the CPU; (Figure 3; item 102) [initiate crisis recovery procedure defines debugging mode]

- Transferring one of the data requests from the local bus to the peripheral bus via the first bridge. (Column 4; line 34-36 [when CPU executes the star up routine stored in item 80 it has to transit by the item 14 (first bridge) to request data. First bridge is located between local and peripheral bus])

- responding via the second bridge to the first data requests on the peripheral bus so that the first BIOS code stored in the ROM is loaded in the CPU; (Column 4; line 50-51)[CPU 12 reads data from EEPROM 80 through item 30 which is second bridge]

- and responding via the debugging system to the second data requests on the peripheral so that second BIOS code stored in the debugging system is loaded in the CPU,(Column 4;line 60-65)[User installs a disk containing proper BIOS program on the floppy disk drive is defined as responding via debugging system to second data request]

wherein the CPU is switched to the debugging mode if responding via the second bridge to the first data requests fails, and the first BIOS code is read or reprogrammed by the debugging system for debugging. (Figure 2 shows that item 30 considered, as a second bridge is located between the CPU 12 and SYSTEM BIOS FLASH ROM item 80. The result of this location is all requests from CPU 12 to item 80 have to transit by the bridge), in addition Anderson discloses in (Column 4; lines 56-67) "The CPU 12 is able to execute the BIOS program stored in the EEPROM 80. If so, the CPU 12 continues with the normal boot process at step 100. If not, the CPU 12 executes a crisis recovery procedure at step 102. As is known in the art, the crisis recovery routine prompts the user to install a disk containing the proper BIOS program on the floppy disk drive. Although the user is preferably prompted to install the disk "

In regard to claims 2, and12 Anderson discloses:

- method as claimed in claim 1, wherein the second BIOS code is programmed by the debugging system. (Column 3; line 13-15) [Since disk containing the correct

BIOS is inserted to item 33 considered in parent claim 1 as part of debugging system, this implies that second BIOS code is programmed by item 33]

In regard to claims 3, and 13 Anderson discloses:

- method as claimed in claim 2, wherein the debugging system comprises: an interface card coupled to the peripheral bus; (Figure 2; item 33)
- and a second computer system coupled to the interface card. (Figure 2; item 24)[Item 24 is network card that is coupled to item 33. Item 24 has the capability to connect to other computer system. Consequently all computer system connected to item 24 would be coupled to item 33]

In regard to claims 6, and 16 Anderson discloses:

method as claimed in claim 1 further comprising the step of:

- when the CPU is switched to the debugging mode, overwriting the first BIOS code in the ROM with the second BIOS code by the debugging system through the second bridge.(Figure 2; second BIOS comes from item 33. In order for CPU to override first BIOS it has to read it from item 30 which in turn has to transit by item 30 considered as second bridge)

In regard to claims 8, and 18

Anderson discloses:

- method as claimed in claim 1, wherein the peripheral and expansion buses are a PCI bus and an ISA bus respectively, (Column 4; line 14)

- and first and second bridges are a north bridge and a south bridge respectively (Figure 2; item 14 north bridge and item 30 south bridge)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson US Patent 6,003,130 in view of Hurd US Patent 6,553,502.

In regard to claims 4, and 14

Anderson discloses initializing a computer system equipped with debugging system.

Anderson does not disclose retrieving and displaying contents of registers.

Hurd teaches retrieving and displaying contents of registers. (Column 10; line 64-65)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of retrieving and displaying register content, as taught by Hurd, into the computer system equipped with debugging system of Anderson. A person of ordinary skill in the art would have been motivated to make this modification because displaying the content of registers would better assist the user and makes the debugging process faster, and more efficient.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, and 17are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson US Patent 6,003,130 in view of Crump US Patent 5,898,843.

In regard to claims 7, and 17

Anderson discloses initializing computer system equipped with debugging system.

Anderson does not disclose an A20 CPU gate switching between normal and debugging modes.

Crump teaches switching between normal and debugging mode by using A20 gate (Column 17; line 41)[on is normal off is debugging]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of switching from normal mode to debugging mode using an A20 gate, as taught by Crump, into the computer system equipped with debugging system of Anderson. A person of ordinary skill in the art would have been motivated to make this modification because A20 gate offers high switching speed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9,10,19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson US Patent 6,003,130 in view of Wong US Patent 6,240,480.

In regard to claims 9, and 19

Anderson discloses initializing computer system equipped with debugging system and retrieving first BIOS code in ROM.

Anderson does not disclose that second bridge responds by decoding address carried in data request.

Wong teaches that a bridge may be equipped to decode addresses (Column 4; line 64) and (Column 5; line 1-3)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of decoding addresses by second bridge, as taught by Wong, into computer system equipped with debugging system of Anderson. A person of ordinary skill in the art would have been motivated to make this modification

because decoding addresses at the bridge level would offer a faster recovery to the system.

In regard to claims 10, and 20

Anderson discloses initializing computer system equipped with debugging system and retrieving second BIOS code.

Anderson does not disclose that second bridge responds by decoding address carried in data request.

Wong teaches that a bridge may be equipped to decode addresses (Column 4; line 64) and (Column 5; line 1-3)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feature of decoding addresses by second bridge, as taught by Wong, into computer system equipped with debugging system of Anderson. A person of ordinary skill in the art would have been motivated to make this modification because decoding addresses at the bridge level would offer a faster recovery to the system.

Response to Applicant's Argument

Applicant arguments filed on July 17, 2006 have been fully considered, and are not persuasive.

In regard to the argument in which the Applicant states, "it is respectfully submitted that Anderson neither discloses nor suggests switching a CPU to a debugging mode

if a first data request that is directed to a ROM fails, whereupon a first BIOS code is read or reprogrammed by a debugging system, in accordance with claim 1. Similarly, Anderson does not teach or suggest that a CPU is switched to a debugging mode if a second bridge fails to respond to a first data request with a first BIOS code, and a debugging system reads or reprograms the first BIOS code for debugging, in accordance with independent claim 11" Examiner respectfully disagrees. Examiner points Applicant to "The CPU 12 is able to execute the BIOS program stored in the EEPROM 80. If so, the CPU 12 continues with the normal boot process at step 100. If not, the CPU 12 executes a crisis recovery procedure at step 102. As is known in the art, the crisis recovery routine prompts the user to install a disk containing the proper BIOS program on the floppy disk drive. Although the user is preferably prompted to install the disk" Examiner considers the execution of the crisis recovery as switching to the debugging mode.

In regard to the second part of the argument, Examiner emphasizes that what is being argued is not included in the claim language. Thus the claim recites "wherein the CPU is switched to the debugging mode **if responding via the second bridge to the first data requests fails**", but the argument states "Anderson does not teach or suggest that a CPU is switched to a debugging mode **if a second bridge fails to respond**" Examiner understands that it is the response via the second bridge which fails not the second bridge itself.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
Amine Riad
Patent Examiner

9/14/2006

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